

## EAST SEARCH

5/15/04

L#	Hits	Search String	Databases
L1	2590	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	187	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L3	181	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and ((encod\$1 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L5	36	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L6	45	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (identic\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L7	0	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (encod\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L8	0	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (encod\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L9	56	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (encod\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L10	14	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (encod\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L11	32	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (identic\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L12	17	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (identic\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L13	1	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and ((encod\$ USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L14	0	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (ternary USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L15	7	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (symbol USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L16	131	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (symbol USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L4	19	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L17	16	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L18	3403	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L20	481	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L21	120	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L22	1	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L23	7	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L25	0	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L26	1	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L27	7	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L31	2	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L32	42	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	
L33	4	((integrated or digital) adj circuit\$1) with (simulation or (model near2 check\$3)) and (reduc\$4 w USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	

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5/15/04

Results of search set L24:(processor\$1 or "processing unit") with ((estimate\$3 or determin\$5 or calculat\$3) near2 electromagnetic)

DocumentKind Codes Title

US 20040070772 A1 Parametric profiling using optical spectroscopic systems

Issue Date

20040415 356/625

Abstract

US 20040040285 A1	Control of oxygen storage in a catalytic converter	20040304 60/285
US 20040024578 A1	Discrete event simulation system and method	20040205 703/17
US 20040012600 A1	Scalable high performance 3d graphics	20040122 345/506
US 20030167135 A1	Non-linear modelling of biological activity of chemical compounds	20030904 702/22
US 20030144828 A1	Hub array system and method	20030731 703/21
US 20030115030 A1	Non-linear modelling of biological activity of chemical compounds	20030619 703/11
US 20030036007 A1	Field correction of overlay error	20030220 430/30
US 20030034570 A1	Field correction of overlay error	20030220 257/797
US 20030022079 A1	Field correction of overlay error	20030130 430/30
US 20030022075 A1	Field correction of overlay error	20030130 430/5
US 20020166891 A1	Systems and methods for deploying a point-of sale device	20021114 235/379
US 20020161566 A1	Method and apparatus for morphological modeling of complex systems to predict performance	20021031 703/21
US 20020152060 A1	Inter-chip communication system	20021017 703/17
US 20020147555 A1	Method and apparatus for analyzing a source current waveform in a semiconductor integrater	20021010 702/70
US 20020113966 A1	Parametric profiling using optical spectroscopic systems	20020822 356/369
US 20020044014 A1	Amplifier measurement and modeling processes for use in generating predistortion parameter	20020418 330/2
US 20020008578 A1	Amplifier measurement and modeling processes for use in generating predistortion parameter	20020124 330/149
US 20010050592 A1	Amplifier measurement and modeling processes for use in generating predistortion parameter	20011213 330/2
US 6697436 B1	Transmission antenna array system with predistortion	20040224 375/296
US 6651225 B1	Dynamic evaluation logic system and method	20031118 716/4
US 6587514 B1	Digital predistortion methods for wideband amplifiers	20030701 375/296
US 6577992 B1	Transistor level circuit simulator using hierarchical data	20030610 703/14
US 6559856 B1	Apparatus for fixed-point graphics and method thereof	20030506 345/600
US 6476670 B2	Amplifier measurement and modeling processes for use in generating predistortion parameter	20021105 330/2
US 6459334 B2	Amplifier measurement and modeling processes for use in generating predistortion parameter	20021001 330/2
US 6440612 B1	Field correction of overlay error	20020827 430/5
US 6421251 B1	Array board interconnect system and method	20020716 361/788
US 6389379 B1	Converfication system and method	20020514 703/14
US 6388513 B1	Amplifier measurement and modeling processes for use in generating predistortion parameter	20020514 330/2
US 6356146 B1	Amplifier measurement and modeling processes for use in generating predistortion parameter	20020312 330/2
US 6342810 B1	Predistortion amplifier system with separately controllable amplifiers	20020129 330/51
US 6321366 B1	Timing-insensitive glitch-free logic system and method	20011120 716/6
US 6134516 A	Simulation server system and method	20001017 703/27
US 6026230 A	Memory simulation system and method	20000215 703/13
US 5850088 A	Teg for carrier lifetime evaluation	19981215 257/48
US 5701024 A	Electrostatic discharge (ESD) protection structure for high voltage pins	19971223 257/360
US 5687068 A	Power supply for in-line power controllers and two-terminal electronic thermostat employing si	19971111 363/126
US 5381343 A	Hier archical pitchmaking compaction method and system for integrated circuit design	19950110 716/2
US 5216354 A	Controllable voltage-to-current converter having third-order distortion reduction	19930601 323/312
US 4802103 A	Brain learning and recognition emulation circuitry and method of recognizing events	19890131 706/38
US 3786219 A	SOLID STATE INDUCTION COOKING SYSTEMS FOR RANGES AND SURFACE COOKING	19740115 219/626